SIG24293: 8000SPS, 24-bit Sigma-Delta ADC with PGA and Reference

FEATURES

Programmable Gain: 1/2/4/8/16/32/64/128
Data Rates: 7.8SPS to 8kSPS
RMS Noise: 24nV at 10SPS (Gain=128)
20.8 noise-free bits at 10SPS (Gain=1)
Offset Drift: 5nV/°C (Gain=128)
Gain Drift: 1ppm/°C
1.17V/2.5V Internal Reference with 4ppm/°C Drift
Integral Non-Linearity: 2ppm
Internal or External Clock
Simultaneous 50Hz/60Hz Rejection
4 Differential/7 Pseudo Differential Inputs
Automatic Channel Sequencer
Programmable Current Sources
On-Chip Bias Voltage Generator
Burnout Current Sources
Parity Check
Power Supply
- **AVDD: 2.7V to 5.25V**
- **DVDD: 2.7V to 5.25V**

Current: 1.3mA
Package: 16-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Temperature Measurement
Industrial Process Control
Pressure Sensors

DESCRIPTION

The SIG24293 is a low noise, low drift, and high-resolution 24-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) and low drift on-chip voltage reference that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

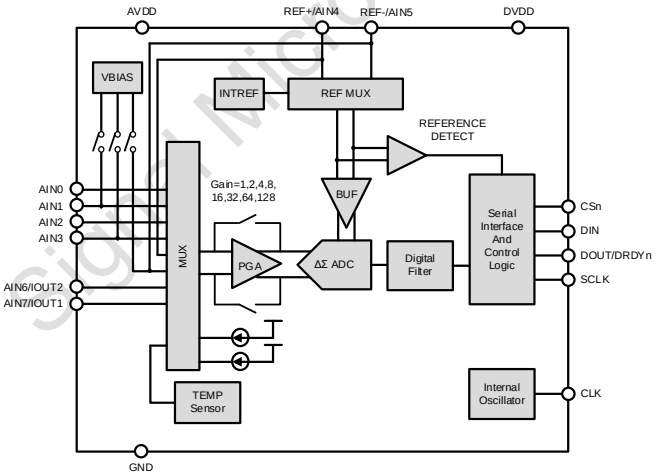
The device contains a low noise PGA with gains selected from 1, 2, 4, 8 16, 32, 64, and 128, a delta-sigma (Δ-Σ) modulator, and a programmable digital SINC4/SINC3/fast settling filter. 50Hz/60Hz simultaneous rejection option is also provided. A low drift 1.17V or 2.5V reference is integrated on chip and two matched excitation current sources (IEXCs) are provided for accurate RTD measurement. The output data rate from the device can be configured from 7.8SPS up to 8000SPS. This device provides channel sequencer feature to measure four differential inputs or seven pseudo differential inputs automatically. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

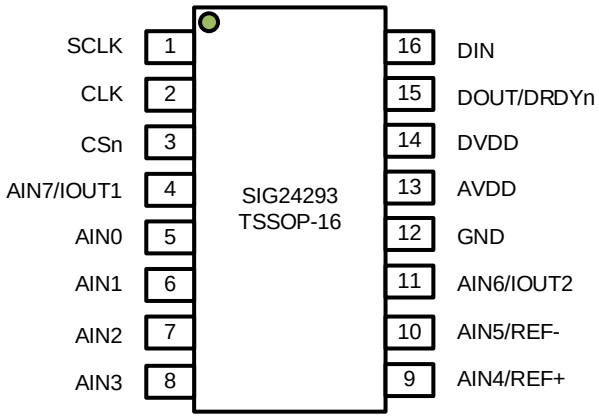
The on-chip oscillator or external clock can be used as the clock source to the device.

The SIG24293 is available in 16-lead TSSOP package and is fully specified over the -40°C to +125°C temperature range.

Function Block Diagram

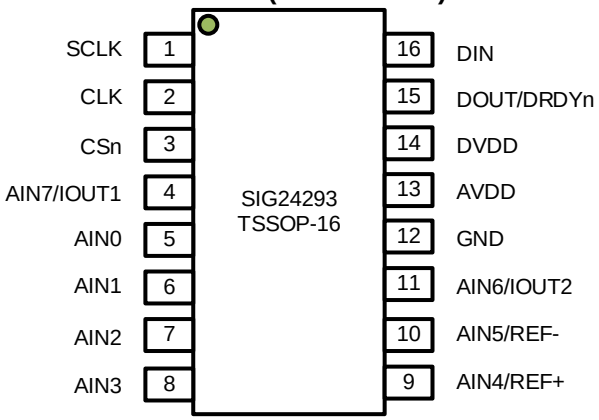


TSSOP-16



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	SCLK	Digital Input	Serial data clock.
2	CLK	Digital Input/Output	Master clock input or internal clock output depending on MODE Register bits CLK[1:0].
3	CSn	Digital Input	Serial chip select. Active low.
4	AIN7/IOUT1	Analog Input/Output	Analog input channel 7 or internal excitation current output 1.
5	AIN0	Analog Input	Analog input channel 0.
6	AIN1	Analog Input	Analog input channel 1.
7	AIN2	Analog Input	Analog input channel 2.
8	AIN3	Analog Input	Analog input channel 3.
9	AIN4/REF+	Analog Input	Analog input channel 4 or positive reference input.
10	AIN5/REF-	Analog Input	Analog input channel 5 or negative reference input.
11	AIN6/IOUT2	Analog Input	Analog input channel 6 or internal excitation current output 2.
12	GND	Analog	Ground reference point.
13	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to GND. AVDD is independent of DVDD.
14	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
15	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.
16	DIN	Digital Input	Serial data input.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG24293	TSSOP-16	-40°C to +125°C	SIG24293-ITSP16-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to GND	–0.3	6.5	V
	DVDD to GND	–0.3	6.5	V
	Analog input	–0.3	V_{AVDD} + 0.3	V
	Digital input	–0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body model	ANSI/ESDA/JEDEC JS-001	±6000	V
MM	Machine model	JEDEC EIA/JESD22-A115C	±400	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{DVDD}=3.3V, V_{GND}=0V, V_{REF}=2.5V, f_{CLK}=4.096MHz, data rate=10SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–V_{REF}$/Gain		$+V_{REF}$/Gain	V
Absolute Input Voltage	Buffer Off	– 0.05		V_{AVDD} + 0.05	V
	Buffer On	+ 0.5		V_{AVDD} – 0.5	
Common Mode Input Range	Buffer On	+ 0.5 + $\lvert V_{INMAX}\rvert$·Gain/2		V_{AVDD} – 0.5 – $\lvert V_{INMAX}\rvert$·Gain/2	V
Absolute Input Current	Buffer off		±10		nA
	Buffer On		±1		nA
SYSTEM PERFORMANCE					
PGA Gain		1/2/4/8/16/32/64/128			V/V
Resolution			24		Bits
Data Rate		7.8		8000	SPS
Noise		See Noise Table			
Integral Nonlinearity (INL)	Buffer Off		±10		ppm
	Buffer On		±2		ppm
Offset Error	Chop Off		±400/Gain		µV
	Chop On		±1		µV
Offset Drift vs. Temperature	All PGA gains		±400/Gain ± 2		nV/°C
Gain Error(2)	Gain = 1, 2, and 4	-100	±20	100	ppm
	Gain = 8, 16, and 32	-150	±50	150	
	Gain = 64, and 128	-250	±100	250	
Gain Mismatch(2)	All PGA gains		150	300	ppm
Gain Drift vs. Temperature	All PGA gains	-3	±1	+3	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN} = 50/60Hz, ±2%, data rate=10SPS		See Table 19		dB
Common Mode Rejection (CMRR)	f_{IN} = 50Hz, data rate = 1000SPS	100	120		dB
Power Supply Rejection(2) (PSRR)	AVDD	85	105		dB
	DVDD	90	110		dB
EXTERNAL REFERENCE INPUTS					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5	2.5	V_{AVDD} + 0.1	V
Absolute Negative Reference Voltage (V_{REFN})		– 0.05		V_{REFP} – 0.5	V
Absolute Positive Reference Voltage (V_{REFP})		V_{REFN} + 0.5		V_{AVDD} + 0.05	V
Average Voltage Input Current			±500		nA
INTERNAL VOLTAGE REFERENCE					
Reference Voltage			1.17/2.5		V
Initial Accuracy(2)		-0.05%	±0.005%	+0.05%	
Temperature Drift		-20	±4	+20	ppm/°C
EXCITATION CURRENT SOURCES (IEXC1 and IEXC2)					
Output Current		10/50/100/210/250/500/1000			µA
Compliance Voltage(3)	IEXC<=250µA	0		V_{AVDD} – 0.5	V
	IEXC=500µA	0		V_{AVDD} – 0.6	
	IEXC=1000µA	0		V_{AVDD} – 0.8	
Accuracy	IEXC=10µA	-4%	±2%	+4%	
	IEXC>=50µA	-2%	±1%	+2%	

Current Mismatch IEXC1=IEXC2	10μA	-3.0%	±0.60%	+3.0%	
	50μA	-1.5%	±0.25%	+1.5%	
	100μA	-1.2%	±0.20%	+1.2%	
	210μA, 250μA	-1.0%	±0.18%	+1.0%	
	500μA	-0.8%	±0.12%	+0.8%	
	1000μA	-0.6%	±0.1%	+0.6%	
Temperature Drift		-90	±20	+90	ppm/°C
Temperature Drift Mismatch		-30	±5	+30	ppm/°C
Burnout Current Sources					
Current Setting			1		μA
ADC CLOCK					
External Clock	Frequency Range	1	4.096	4.1	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		4.096		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	$0.8 \cdot V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			$0.2 \cdot V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7 \cdot V_{DVDD}$		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		V_{DGND}		$0.3 \cdot V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				±10	μA
POWER SUPPLY					
AVDD Voltage (V_{AVDD})		2.7		5.25	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD Current (I_{AVDD})	Buffer Off		440	600	μA
	Buffer On		900	1200	μA
	Sleep Mode		1		μA
	Power-down Mode		1		μA
DVDD Current (I_{DVDD})	Active Mode		370	500	μA
	Sleep Mode		22		μA
	Power-down Mode		1		μA
Total Power Dissipation	Buffer Off		3.2		mW
	Buffer On		5.5		mW
	Sleep Mode		0.07		mW
	Power-down Mode		0.01		mW
TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) MIN and MAX values listed for gain error are for +25˚C room temperature only.
(3) The IDAC current does not change by more than 0.01% from the nominal value when staying within the specified compliance voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

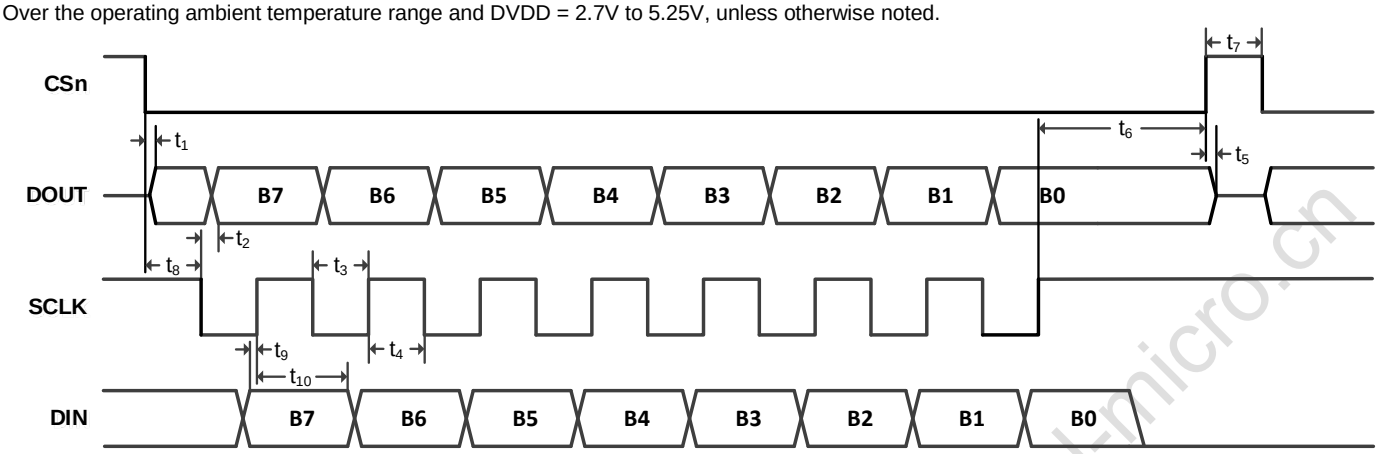


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to DOUT/DRDYn driven: propagation delay(1)		50	ns
t_2	SCLK falling edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK low pulse width	100		ns
t_4	SCLK high pulse width	100		ns
	SCLK period	200	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		40	ns
t_6	Last SCLK rising edge to CSn rising edge: delay time	50		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK falling edge: setup time(2)	50		ns
t_9	Valid DIN to SCLK rising edge: setup time	50		ns
t_{10}	Valid DIN to SCLK rising edge: hold time	25		ns

(1) DOUT load = 20pF || 100kΩ to DGND.
(2) CSn can be tied low.

NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC4 and SINC3 filters and fast settling mode with chop disabled. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF}/\text{Gain}/V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF}/\text{Gain}/V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V. With chop enabled, the resolution improves by 0.5 bits.

External Reference and SINC4 Filter

Table 1. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	0.427(2.38)	0.228(1.28)	0.143(0.787)	0.080(0.408)	0.043(0.219)	0.031(0.161)	0.025(0.147)	0.022(0.123)
800	10	0.478(2.66)	0.255(1.43)	0.160(0.880)	0.089(0.457)	0.048(0.245)	0.034(0.181)	0.028(0.164)	0.024(0.137)
400	20	0.675(3.76)	0.361(2.02)	0.226(1.24)	0.126(0.646)	0.067(0.346)	0.048(0.255)	0.039(0.232)	0.034(0.194)
160	50	1.07(5.94)	0.571(3.19)	0.357(1.97)	0.199(1.02)	0.107(0.548)	0.076(0.404)	0.062(0.367)	0.054(0.306)
133	60	1.17(6.51)	0.626(3.50)	0.392(2.16)	0.218(1.12)	0.117(0.600)	0.084(0.442)	0.068(0.402)	0.059(0.336)
80	100	1.51(8.40)	0.808(4.52)	0.506(2.78)	0.282(1.44)	0.151(0.774)	0.108(0.571)	0.088(0.518)	0.077(0.433)
64	125	1.69(9.39)	0.903(5.05)	0.565(3.11)	0.315(1.61)	0.169(0.866)	0.121(0.638)	0.098(0.580)	0.086(0.484)
40	200	2.14(11.9)	1.14(6.39)	0.715(3.94)	0.398(2.04)	0.213(1.10)	0.153(0.807)	0.124(0.733)	0.108(0.613)
32	250	2.36(14.0)	1.42(9.21)	0.782(4.38)	0.375(2.30)	0.270(1.52)	0.168(0.937)	0.128(0.789)	0.123(0.722)
20	400	3.06(17.8)	1.68(8.91)	0.983(6.16)	0.872(6.39)	0.326(1.73)	0.215(1.25)	0.171(0.993)	0.147(0.817)
16	500	3.05(16.6)	1.96(13.7)	1.10(7.05)	0.601(3.82)	0.366(2.06)	0.228(1.36)	0.184(1.07)	0.162(1.07)
10	800	4.46(27.3)	2.50(16.3)	1.28(8.98)	0.781(4.83)	0.476(2.78)	0.298(1.78)	0.232(1.56)	0.208(1.26)
8	1000	4.54(30.6)	2.77(18.0)	1.52(10.1)	0.844(5.31)	0.498(3.12)	0.343(2.23)	0.271(1.85)	0.246(1.45)
4	2000	6.69(44.6)	3.91(25.8)	2.09(15.5)	1.19(8.39)	0.714(4.55)	0.488(3.18)	0.373(2.55)	0.352(2.29)
2	4000	9.60(64.7)	5.71(38.2)	3.07(21.7)	1.69(11.7)	1.01(7.33)	0.694(5.48)	0.531(3.88)	0.476(3.41)
1	8000	30.9(249)	16.6(120)	8.36(92.1)	4.16(46.2)	2.28(19.0)	1.30(10.0)	0.872(6.31)	0.709(5.38)

Table 2. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	23.5(21.0)	23.4(20.9)	23.1(20.6)	22.9(20.5)	22.8(20.4)	22.3(19.9)	21.6(19.0)	20.8(18.3)
800	10	23.3(20.8)	23.2(20.7)	22.9(20.4)	22.7(20.4)	22.6(20.3)	22.1(19.7)	21.4(18.9)	20.6(18.1)
400	20	22.8(20.3)	22.7(20.2)	22.4(19.9)	22.2(19.9)	22.1(19.8)	21.6(19.2)	20.9(18.4)	20.1(17.6)
160	50	22.2(19.7)	22.1(19.6)	21.7(19.3)	21.6(19.2)	21.5(19.1)	21.0(18.6)	20.3(17.7)	19.5(17.0)
133	60	22.0(19.6)	21.9(19.4)	21.6(19.1)	21.4(19.1)	21.4(19.0)	20.8(18.4)	20.1(17.6)	19.3(16.8)
80	100	21.7(19.2)	21.6(19.1)	21.2(18.8)	21.1(18.7)	21.0(18.6)	20.5(18.1)	19.8(17.2)	19.0(16.5)
64	125	21.5(19.0)	21.4(18.9)	21.1(18.6)	20.9(18.6)	20.8(18.5)	20.3(17.9)	19.6(17.0)	18.8(16.3)
40	200	21.2(18.7)	21.1(18.6)	20.7(18.3)	20.6(18.2)	20.5(18.1)	20.0(17.6)	19.3(16.7)	18.5(16.0)
32	250	21.0(18.5)	20.7(18.1)	20.6(18.1)	20.7(18.1)	20.1(17.6)	19.8(17.3)	19.2(16.6)	18.3(15.7)
20	400	20.6(18.1)	20.5(18.1)	20.3(17.6)	19.5(16.6)	19.9(17.5)	19.5(16.9)	18.8(16.3)	18.0(15.5)
16	500	20.6(18.2)	20.3(17.5)	20.1(17.4)	20.0(17.3)	19.7(17.2)	19.4(16.8)	18.7(16.2)	17.9(15.2)
10	800	20.1(17.5)	19.9(17.2)	19.9(17.1)	19.6(17.0)	19.3(16.8)	19.0(16.4)	18.4(15.6)	17.5(14.9)
8	1000	20.1(17.3)	19.8(17.1)	19.6(16.9)	19.5(16.8)	19.3(16.6)	18.8(16.1)	18.1(15.4)	17.3(14.7)
4	2000	19.5(16.8)	19.3(16.6)	19.2(16.3)	19.0(16.2)	18.7(16.1)	18.3(15.6)	17.7(14.9)	16.8(14.1)
2	4000	19.0(16.2)	18.7(16.0)	18.6(15.8)	18.5(15.7)	18.2(15.4)	17.8(14.8)	17.2(14.3)	16.3(13.5)

External Reference and SINC3 Filter

Table 3. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	0.468(2.44)	0.263(1.34)	0.147(1.01)	0.088(0.490)	0.047(0.238)	0.033(0.189)	0.027(0.161)	0.023(0.128)
800	10	0.523(2.73)	0.294(1.49)	0.164(1.13)	0.098(0.548)	0.053(0.266)	0.037(0.212)	0.030(0.181)	0.026(0.143)
400	20	0.740(3.85)	0.416(2.11)	0.232(1.60)	0.138(0.775)	0.074(0.376)	0.052(0.299)	0.043(0.255)	0.036(0.203)
160	50	1.17(6.09)	0.658(3.34)	0.367(2.52)	0.219(1.23)	0.118(0.594)	0.083(0.473)	0.068(0.404)	0.057(0.320)
133	60	1.28(6.68)	0.720(3.66)	0.402(2.77)	0.240(1.34)	0.129(0.651)	0.091(0.519)	0.075(0.442)	0.063(0.351)
80	100	1.66(8.62)	0.930(4.73)	0.519(3.57)	0.310(1.73)	0.166(0.840)	0.117(0.669)	0.096(0.571)	0.081(0.453)
64	125	1.85(9.64)	1.04(5.28)	0.581(3.99)	0.346(1.94)	0.186(0.939)	0.131(0.748)	0.108(0.638)	0.091(0.506)
40	200	2.34(12.2)	1.32(6.68)	0.734(5.05)	0.438(2.45)	0.235(1.19)	0.166(0.947)	0.136(0.807)	0.114(0.640)
32	250	2.60(13.4)	1.54(8.32)	0.789(4.46)	0.453(2.45)	0.264(1.45)	0.178(0.956)	0.140(0.738)	0.135(0.828)
20	400	3.17(16.9)	1.88(12.3)	1.02(5.79)	0.568(3.94)	0.331(2.04)	0.239(1.34)	0.177(0.956)	0.167(0.993)
16	500	3.26(21.1)	2.07(11.6)	1.10(6.98)	0.660(3.97)	0.386(2.38)	0.268(1.97)	0.195(1.10)	0.173(0.998)
10	800	4.48(28.2)	2.71(17.2)	1.42(8.61)	0.816(4.60)	0.471(3.27)	0.317(2.35)	0.262(1.66)	0.238(1.29)
8	1000	4.89(30.9)	2.95(19.6)	1.62(11.8)	0.868(5.72)	0.549(3.77)	0.369(2.21)	0.275(1.83)	0.257(1.62)
4	2000	8.28(53.5)	4.68(32.1)	2.51(17.4)	1.43(10.5)	0.799(5.68)	0.516(3.33)	0.410(3.15)	0.370(2.89)
2	4000	35.7(205)	18.3(108)	9.21(54.2)	4.60(26.0)	2.44(15.4)	1.32(8.44)	0.780(5.19)	0.575(4.01)
1	8000	273(1520)	137(748)	68.4(386)	34.4(196)	17.2(97.9)	8.55(49.7)	4.41(28.2)	2.23(13.5)

Table 4. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	23.3(21.0)	23.2(20.8)	23.0(20.2)	22.8(20.3)	22.7(20.3)	22.2(19.7)	21.5(18.9)	20.7(18.2)
800	10	23.2(20.8)	23.0(20.7)	22.9(20.1)	22.6(20.1)	22.5(20.2)	22.0(19.5)	21.3(18.7)	20.5(18.1)
400	20	22.7(20.3)	22.5(20.2)	22.4(19.6)	22.1(19.6)	22.0(19.7)	21.5(19.0)	20.8(18.2)	20.0(17.6)
160	50	22.0(19.6)	21.9(19.5)	21.7(18.9)	21.4(19.0)	21.3(19.0)	20.8(18.3)	20.1(17.6)	19.4(16.9)
133	60	21.9(19.5)	21.7(19.4)	21.6(18.8)	21.3(18.8)	21.2(18.9)	20.7(18.2)	20.0(17.4)	19.2(16.8)
80	100	21.5(19.1)	21.4(19.0)	21.2(18.4)	20.9(18.5)	20.8(18.5)	20.3(17.8)	19.6(17.1)	18.9(16.4)
64	125	21.4(19.0)	21.2(18.9)	21.0(18.3)	20.8(18.3)	20.7(18.3)	20.2(17.7)	19.5(16.9)	18.7(16.2)
40	200	21.0(18.6)	20.9(18.5)	20.7(17.9)	20.4(18.0)	20.3(18.0)	19.8(17.3)	19.1(16.6)	18.4(15.9)
32	250	20.9(18.5)	20.6(18.2)	20.6(18.1)	20.4(18.0)	20.2(17.7)	19.7(17.3)	19.1(16.7)	18.1(15.5)
20	400	20.6(18.2)	20.3(17.6)	20.2(17.7)	20.1(17.3)	19.8(17.2)	19.3(16.8)	18.8(16.3)	17.8(15.3)
16	500	20.5(17.9)	20.2(17.7)	20.1(17.5)	19.9(17.3)	19.6(17.0)	19.2(16.3)	18.6(16.1)	17.8(15.3)
10	800	20.1(17.4)	19.8(17.1)	19.7(17.1)	19.5(17.1)	19.3(16.5)	18.9(16.0)	18.2(15.5)	17.3(14.9)
8	1000	20.0(17.3)	19.7(17.0)	19.6(16.7)	19.5(16.7)	19.1(16.3)	18.7(16.1)	18.1(15.4)	17.2(14.6)
4	2000	19.2(16.5)	19.0(16.3)	18.9(16.1)	18.7(15.9)	18.6(15.7)	18.2(15.5)	17.5(14.6)	16.7(13.7)
2	4000	17.1(14.6)	17.1(14.5)	17.1(14.5)	17.1(14.6)	17.0(14.3)	16.9(14.2)	16.6(13.9)	16.1(13.2)
1	8000	14.2(11.7)	14.2(11.7)	14.2(11.7)	14.1(11.6)	14.2(11.6)	14.2(11.6)	14.1(11.4)	14.1(11.5)

Internal Reference and SINC4 Filter

Table 5. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, Internal 2.5V Reference, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	1.30(6.69)	0.667(3.55)	0.350(1.93)	0.179(1.01)	0.082(0.434)	0.052(0.256)	0.031(0.164)	0.022(0.118)
800	10	1.45(7.48)	0.746(3.97)	0.392(2.16)	0.200(1.13)	0.092(0.486)	0.058(0.286)	0.035(0.184)	0.024(0.132)
400	20	2.05(10.6)	1.05(5.62)	0.554(3.06)	0.282(1.60)	0.129(0.687)	0.082(0.405)	0.049(0.260)	0.035(0.187)
160	50	3.24(16.7)	1.67(8.88)	0.876(4.83)	0.446(2.52)	0.205(1.09)	0.130(0.640)	0.077(0.411)	0.055(0.296)
133	60	3.55(18.3)	1.83(9.73)	0.959(5.30)	0.489(2.77)	0.224(1.19)	0.142(0.702)	0.085(0.450)	0.060(0.324)
80	100	4.59(23.7)	2.36(12.6)	1.24(6.84)	0.631(3.57)	0.290(1.54)	0.184(0.906)	0.109(0.581)	0.077(0.418)
64	125	5.13(26.5)	2.64(14.0)	1.38(7.64)	0.706(3.99)	0.324(1.72)	0.205(1.01)	0.122(0.649)	0.086(0.468)
40	200	6.49(33.5)	3.34(17.8)	1.75(9.67)	0.893(5.05)	0.409(2.17)	0.260(1.28)	0.154(0.821)	0.109(0.592)
32	250	6.70(37.4)	3.85(19.6)	1.87(11.1)	0.987(5.05)	0.476(2.52)	0.286(1.64)	0.182(1.06)	0.146(0.777)
20	400	8.82(61.2)	4.97(28.1)	2.67(15.0)	1.29(7.54)	0.639(3.53)	0.407(2.64)	0.229(1.50)	0.166(0.933)
16	500	10.5(54.9)	5.53(37.0)	2.66(15.7)	1.41(8.17)	0.698(4.23)	0.398(2.71)	0.234(1.45)	0.183(0.979)
10	800	13.1(74.8)	6.60(40.5)	3.35(24.4)	1.73(11.0)	0.896(5.64)	0.482(3.20)	0.318(1.97)	0.246(1.54)
8	1000	15.2(89.1)	7.41(48.9)	3.81(26.1)	1.93(12.5)	1.03(6.31)	0.574(3.61)	0.352(2.19)	0.264(1.70)
4	2000	21.1(136)	10.7(79.3)	5.41(33.6)	2.80(19.5)	1.45(11.2)	0.769(5.18)	0.496(3.94)	0.374(2.35)
2	4000	29.8(219)	15.2(110)	7.90(53.7)	3.91(28.7)	2.03(13.8)	1.15(9.30)	0.706(4.84)	0.525(3.91)
1	8000	51.0(413)	25.4(215)	13.0(114)	6.59(53.6)	3.39(25.0)	1.80(14.1)	1.07(7.89)	0.789(5.32)

Table 6. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, Internal 2.5V Reference, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	21.9(19.5)	21.8(19.4)	21.8(19.3)	21.7(19.2)	21.9(19.5)	21.5(19.2)	21.3(18.9)	20.8(18.3)
800	10	21.7(19.3)	21.7(19.3)	21.6(19.1)	21.6(19.1)	21.7(19.3)	21.4(19.1)	21.1(18.7)	20.6(18.2)
400	20	21.2(18.8)	21.2(18.8)	21.1(18.6)	21.1(18.6)	21.2(18.8)	20.9(18.6)	20.6(18.2)	20.1(17.7)
160	50	20.6(18.2)	20.5(18.1)	20.4(18.0)	20.4(17.9)	20.5(18.1)	20.2(17.9)	19.9(17.5)	19.4(17.0)
133	60	20.4(18.1)	20.4(18.0)	20.3(17.8)	20.3(17.8)	20.4(18.0)	20.1(17.8)	19.8(17.4)	19.3(16.9)
80	100	20.1(17.7)	20.0(17.6)	19.9(17.5)	19.9(17.4)	20.0(17.6)	19.7(17.4)	19.4(17.0)	18.9(16.5)
64	125	19.9(17.5)	19.9(17.4)	19.8(17.3)	19.8(17.3)	19.9(17.5)	19.5(17.2)	19.3(16.9)	18.8(16.3)
40	200	19.6(17.2)	19.5(17.1)	19.4(17.0)	19.4(16.9)	19.5(17.1)	19.2(16.9)	18.9(16.5)	18.4(16.0)
32	250	19.5(17.0)	19.3(17.0)	19.3(16.8)	19.3(16.9)	19.3(16.9)	19.1(16.5)	18.7(16.2)	18.0(15.6)
20	400	19.1(16.3)	18.9(16.4)	18.8(16.3)	18.9(16.3)	18.9(16.4)	18.5(15.9)	18.4(15.7)	17.8(15.4)
16	500	18.9(16.5)	18.8(16.0)	18.8(16.3)	18.8(16.2)	18.8(16.2)	18.6(15.8)	18.3(15.7)	17.7(15.3)
10	800	18.5(16.0)	18.5(15.9)	18.5(15.6)	18.5(15.8)	18.4(15.8)	18.3(15.6)	17.9(15.3)	17.3(14.6)
8	1000	18.3(15.8)	18.4(15.6)	18.3(15.5)	18.3(15.6)	18.2(15.6)	18.1(15.4)	17.8(15.1)	17.2(14.5)
4	2000	17.9(15.2)	17.8(14.9)	17.8(15.2)	17.8(15.0)	17.7(14.8)	17.6(14.9)	17.3(14.3)	16.7(14.0)
2	4000	17.4(14.5)	17.3(14.5)	17.3(14.5)	17.3(14.4)	17.2(14.5)	17.0(14.0)	16.8(14.0)	16.2(13.3)
1	8000	16.6(13.6)	16.6(13.5)	16.6(13.4)	16.5(13.5)	16.5(13.6)	16.4(13.4)	16.2(13.3)	15.6(12.8)

Internal Reference and SINC3 Filter

Table 7. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, Internal 2.5V Reference, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	1.43(7.90)	0.733(3.95)	0.410(2.18)	0.183(0.928)	0.101(0.605)	0.054(0.284)	0.034(0.181)	0.025(0.135)
800	10	1.60(8.83)	0.819(4.42)	0.459(2.44)	0.204(1.04)	0.112(0.677)	0.060(0.318)	0.038(0.202)	0.028(0.151)
400	20	2.27(12.5)	1.16(6.25)	0.649(3.45)	0.289(1.47)	0.159(0.957)	0.085(0.449)	0.054(0.286)	0.039(0.214)
160	50	3.58(19.8)	1.83(9.88)	1.03(5.46)	0.456(2.32)	0.251(1.51)	0.135(0.710)	0.085(0.452)	0.062(0.338)
133	60	3.93(21.6)	2.01(10.8)	1.12(5.98)	0.500(2.54)	0.275(1.66)	0.148(0.778)	0.094(0.496)	0.068(0.370)
80	100	5.07(27.9)	2.59(14.0)	1.45(7.72)	0.645(3.28)	0.356(2.14)	0.191(1.00)	0.121(0.640)	0.088(0.477)
64	125	5.67(31.2)	2.90(15.6)	1.62(8.63)	0.721(3.67)	0.397(2.39)	0.213(1.12)	0.135(0.715)	0.099(0.534)
40	200	7.17(39.5)	3.66(19.8)	2.05(10.9)	0.913(4.64)	0.503(3.03)	0.270(1.42)	0.171(0.905)	0.125(0.675)
32	250	8.59(52.6)	4.03(23.5)	2.14(11.7)	0.990(5.16)	0.542(3.27)	0.312(1.81)	0.195(1.21)	0.147(0.961)
20	400	9.75(59.4)	4.83(29.1)	2.65(14.1)	1.38(8.50)	0.698(4.27)	0.378(2.39)	0.227(1.42)	0.181(1.10)
16	500	11.3(71.9)	5.84(38.0)	2.92(17.6)	1.55(9.80)	0.796(4.88)	0.420(2.49)	0.246(1.49)	0.200(1.19)
10	800	13.6(84.1)	7.49(42.8)	3.70(20.6)	1.82(11.1)	0.977(6.94)	0.558(3.08)	0.332(2.20)	0.256(1.58)
8	1000	15.9(106)	8.08(47.7)	4.05(27.2)	2.01(13.0)	1.10(6.94)	0.602(3.70)	0.383(2.48)	0.287(1.81)
4	2000	23.1(155)	11.8(78.1)	5.94(44.1)	2.94(22.9)	1.54(11.0)	0.856(6.03)	0.533(3.96)	0.396(2.79)
2	4000	47.3(325)	24.1(176)	12.1(78.9)	6.02(38.8)	3.10(19.5)	1.62(11.6)	0.908(6.23)	0.629(4.43)
1	8000	281(1700)	140(803)	69.4(401)	0.868(6.24)	17.1(105)	8.72(50.1)	4.35(28.4)	2.27(14.0)

Table 8. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, Internal 2.5V Reference, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
1000	8	21.7(19.3)	21.7(19.3)	21.5(19.1)	21.7(19.4)	21.6(19.0)	21.5(19.1)	21.1(18.7)	20.6(18.1)
800	10	21.6(19.1)	21.5(19.1)	21.4(19.0)	21.5(19.2)	21.4(18.8)	21.3(18.9)	21.0(18.6)	20.4(18.0)
400	20	21.1(18.6)	21.0(18.6)	20.9(18.5)	21.0(18.7)	20.9(18.3)	20.8(18.4)	20.5(18.1)	19.9(17.5)
160	50	20.4(17.9)	20.4(17.9)	20.2(17.8)	20.4(18.0)	20.2(17.7)	20.1(17.7)	19.8(17.4)	19.3(16.8)
133	60	20.3(17.8)	20.2(17.8)	20.1(17.7)	20.3(17.9)	20.1(17.5)	20.0(17.6)	19.7(17.3)	19.1(16.7)
80	100	19.9(17.4)	19.9(17.4)	19.7(17.3)	19.9(17.5)	19.7(17.2)	19.6(17.2)	19.3(16.9)	18.8(16.3)
64	125	19.8(17.3)	19.7(17.3)	19.6(17.1)	19.7(17.4)	19.6(17.0)	19.5(17.1)	19.1(16.7)	18.6(16.2)
40	200	19.4(16.9)	19.4(16.9)	19.2(16.8)	19.4(17.0)	19.2(16.7)	19.1(16.7)	18.8(16.4)	18.3(15.8)
32	250	19.2(16.5)	19.2(16.7)	19.2(16.7)	19.3(16.9)	19.1(16.5)	18.9(16.4)	18.6(16.0)	18.0(15.3)
20	400	19.0(16.4)	19.0(16.4)	18.9(16.4)	18.8(16.2)	18.8(16.2)	18.7(16.0)	18.4(15.7)	17.7(15.1)
16	500	18.8(16.1)	18.7(16.0)	18.7(16.1)	18.6(16.0)	18.6(16.0)	18.5(15.9)	18.3(15.7)	17.6(15.0)
10	800	18.5(15.9)	18.3(15.8)	18.4(15.9)	18.4(15.8)	18.3(15.5)	18.1(15.6)	17.8(15.1)	17.2(14.6)
8	1000	18.3(15.5)	18.2(15.7)	18.2(15.5)	18.2(15.6)	18.1(15.5)	18.0(15.4)	17.6(14.9)	17.1(14.4)
4	2000	17.7(15.0)	17.7(15.0)	17.7(14.8)	17.7(14.7)	17.6(14.8)	17.5(14.7)	17.2(14.3)	16.6(13.8)
2	4000	16.7(13.9)	16.7(13.8)	16.7(14.0)	16.7(14.0)	16.6(14.0)	16.6(13.7)	16.4(13.6)	15.9(13.1)
1	8000	14.1(11.5)	14.1(11.6)	14.1(11.6)	19.5(16.6)	14.2(11.5)	14.1(11.6)	14.1(11.4)	14.1(11.4)

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please contact to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jul. 20, 2020		Initial release.

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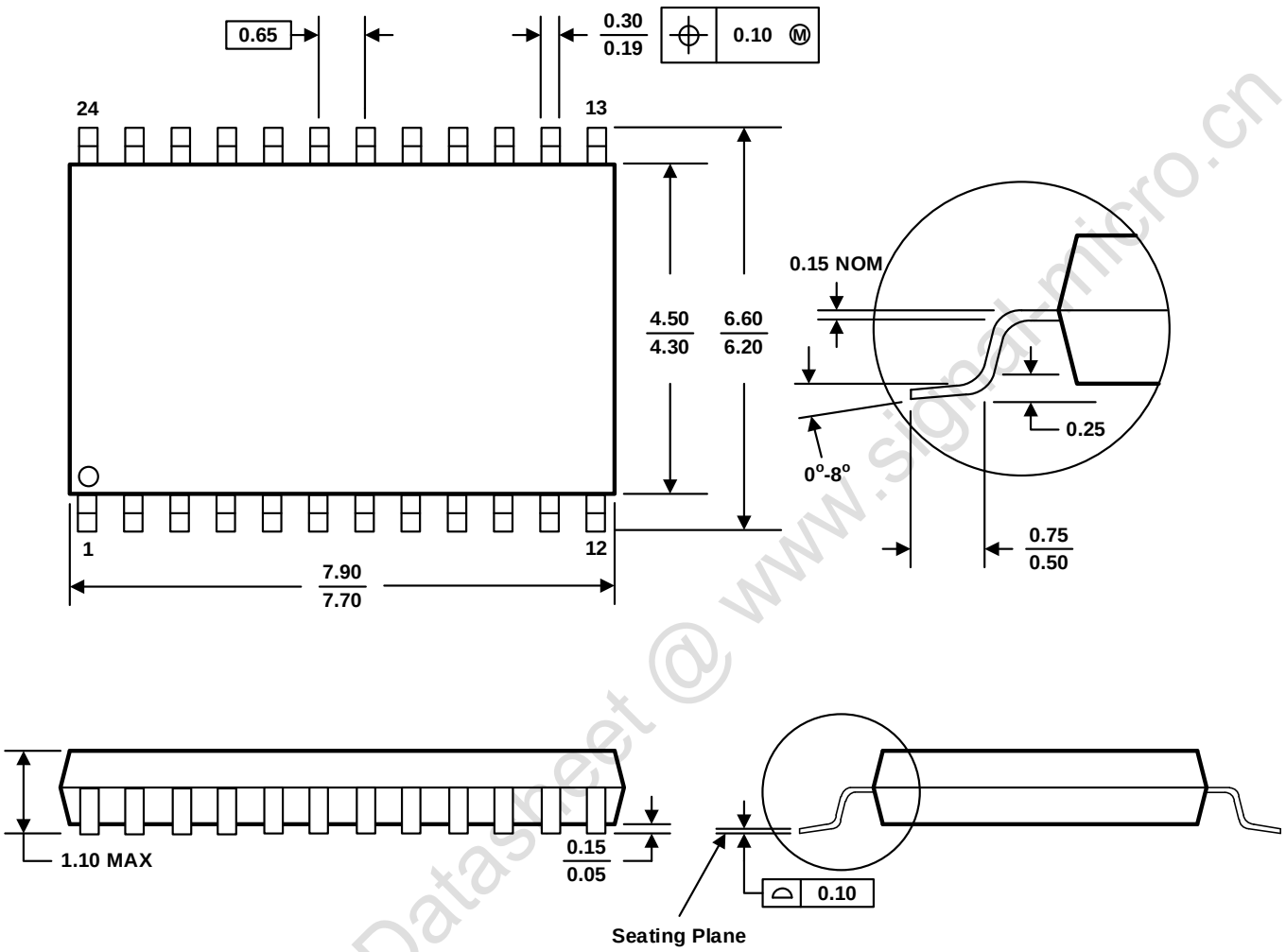
PACKAGE OUTLINE DIMENSIONS



A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.