# 2.5 to 9600SPS, 16-bit Sigma-Delta ADC with PGA and Voltage Reference

## FEATURES

**Programmable Gain: 1/2/4/8/16/32/64/128/256**
**Data Rates: 2.5 to 9600SPS**
**16.0 Noise Free of Bits at 2400SPS (Gain=1)**
**Offset Drift: 5nV/°C (Gain=128)**
**Gain Drift: 1ppm/°C**
**1.17V/2.5V Internal Reference with 5ppm/°C Drift**
**Integral Non-Linearity: 3ppm**
**Internal or External Clock**
**Simultaneous 50Hz/60Hz Rejection**
**Programmable Current Sources**
**On-Chip Bias Voltage Generator**
**Burnout Current Sources**
**Parity Check**
**Power Supply**
- **AVDD: 2.7V to 5.25V or ±2.5V**
- **DVDD: 2.7V to 5.25V**

**Current: 800μA**
**Package: 16/20/24-lead TSSOP**

## APPLICATIONS

**Weigh Scales**
**Strain Gauges**
**Pressure Sensors**
**Temperature Measurement**
**Industrial Process Control**

## DESCRIPTION

The SIG16130/1/2 are low noise, low drift, and high-resolution 16-bit analog-to-digital converters (ADC) with integrated programmable gain amplifier (PGA) and low drift on-chip voltage reference that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

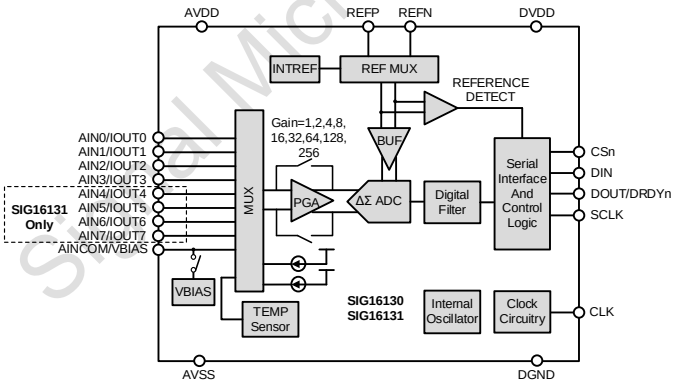
The device contains a low noise PGA with gains selected from 1, 2, 4, 8 16, 32, 64, 128, and 256, a delta-sigma (Δ-Σ) modulator, and a programmable SINC1/SINC4 digital filter. A low drift 1.17V or 2.5V reference is integrated on chip and two matched excitation current sources (IDACs) are provided for accurate RTD measurement. The output data rate from the device can be configured to 2.5 to 9600SPS. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

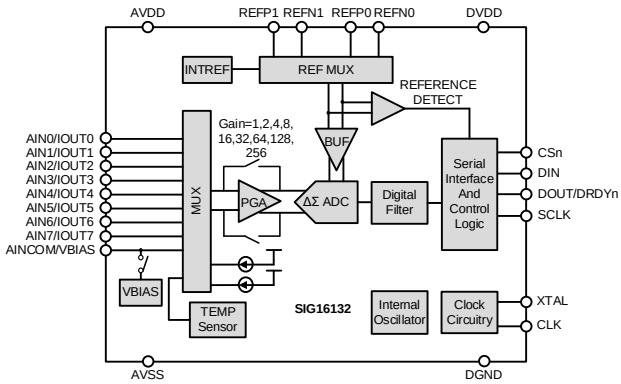
Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

The on-chip oscillator or an external clock can be used as the clock source to the device.

The device can operate with bipolar ±1.35V to ±2.625V analog power supplies, or with a single 2.7V to 5.25V analog power supply.

The SIG16130 is available in 16-lead TSSOP package, the SIG16131 is available in 20-lead TSSOP package, and the SIG16132 is available in 24-lead TSSOP package. All three devices are fully specified over the -40°C to +125°C temperature range.

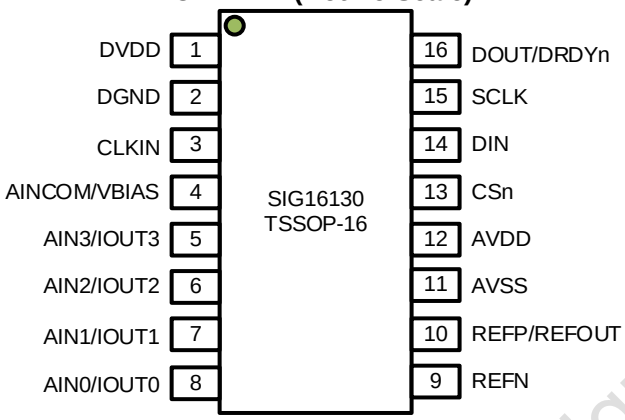


# PIN CONFIGURATION and DESCRIPTIONS

## SIG16130

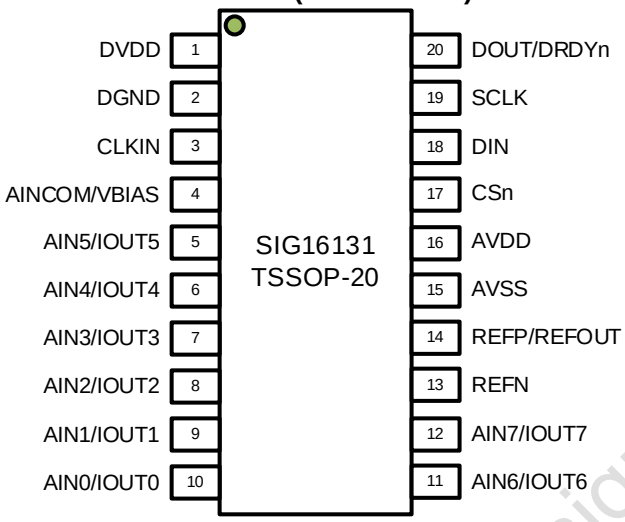
**TOP VIEW (Not To Scale)**




| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DVDD | Digital | Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD. |
| 2 | DGND | Digital | Digital ground reference point. |
| 3 | CLKIN | Digital Input | 1) Internal oscillator: Connect to DGND.<br>2) External clock: Connect to external clock input. |
| 4 | AINCOM/VBIAS | Analog Input | Analog input common, VBIAS. |
| 5 | AIN3/IOUT3 | Analog Input | Analog input 3, IDAC3. |
| 6 | AIN2/IOUT2 | Analog Input | Analog input 2, IDAC2. |
| 7 | AIN1/IOUT1 | Analog Input | Analog input 1, IDAC1. |
| 8 | AIN0/IOUT0 | Analog Input | Analog input 0, IDAC0. |
| 9 | REFN | Analog Input | Negative reference input. |
| 10 | REFP/REFOUT | Analog Input | Positive reference input or internal reference output. |
| 11 | AVSS | Analog | Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to –2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC. |
| 12 | AVDD | Analog | Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD. |
| 13 | CSn | Digital Input | Serial chip select. Active low. |
| 14 | DIN | Digital Input | Serial data input. |
| 15 | SCLK | Digital Input | Serial data clock. |
| 16 | DOUT/DRDYn | Digital Output | Serial data output and data ready indicator. |

## SIG16131

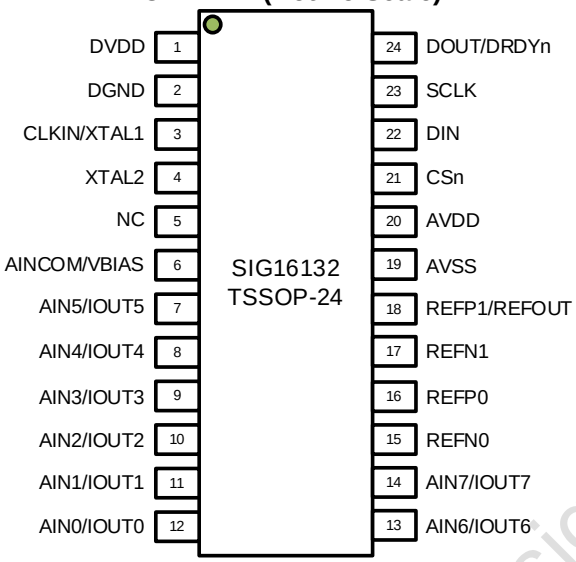
**TOP VIEW (Not To Scale)**




| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DVDD | Digital | Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD. |
| 2 | DGND | Digital | Digital ground reference point. |
| 3 | CLKIN | Digital Input | 1) Internal oscillator: Connect to DGND.<br>2) External clock: Connect to external clock input. |
| 4 | AINCOM/VBIAS | Analog Input | Analog input common, VBIAS. |
| 5 | AIN5/IOUT5 | Analog Input | Analog input 5, IDAC5. |
| 6 | AIN4/IOUT4 | Analog Input | Analog input 4, IDAC4. |
| 7 | AIN3/IOUT3 | Analog Input | Analog input 3, IDAC3. |
| 8 | AIN2/IOUT2 | Analog Input | Analog input 2, IDAC2. |
| 9 | AIN1/IOUT1 | Analog Input | Analog input 1, IDAC1. |
| 10 | AIN0/IOUT0 | Analog Input | Analog input 0, IDAC0. |
| 11 | AIN6/IOUT6 | Analog Input | Analog input 6, IDAC6. |
| 12 | AIN7/IOUT7 | Analog Input | Analog input 7, IDAC7. |
| 13 | REFN | Analog Input | Negative reference input. |
| 14 | REFP/REFOUT | Analog Input | Positive reference input or internal reference output. |
| 15 | AVSS | Analog | Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to –2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC. |
| 16 | AVDD | Analog | Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD. |
| 17 | CSn | Digital Input | Serial chip select. Active low. |
| 18 | DIN | Digital Input | Serial data input. |
| 19 | SCLK | Digital Input | Serial data clock. |
| 20 | DOUT/DRDYn | Digital Output | Serial data output and data ready indicator. |

## SIG16132

**TOP VIEW (Not To Scale)**




| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | DVDD | Digital | Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD. |
| 2 | DGND | Digital | Digital ground reference point. |
| 3 | CLKIN/XTAL1 | Digital Input | 1) Internal oscillator: Connect to DGND.<br>2) External clock: Connect to external clock input.<br>3) Crystal oscillator connection 1. |
| 4 | XTAL2 | Digital Input | Crystal oscillator connection 2. |
| 5 | NC | Digital | No connection (float) or connect to DVDD/DGND. |
| 6 | AINCOM/VBIAS | Analog Input | Analog input common, VBIAS. |
| 7 | AIN5/IOUT5 | Analog Input | Analog input 5, IDAC5. |
| 8 | AIN4/IOUT4 | Analog Input | Analog input 4, IDAC4. |
| 9 | AIN3/IOUT3 | Analog Input | Analog input 3, IDAC3. |
| 10 | AIN2/IOUT2 | Analog Input | Analog input 2, IDAC2. |
| 11 | AIN1/IOUT1 | Analog Input | Analog input 1, IDAC1. |
| 12 | AIN0/IOUT0 | Analog Input | Analog input 0, IDAC0. |
| 13 | AIN6/IOUT6 | Analog Input | Analog input 6, IDAC6. |
| 14 | AIN7/IOUT7 | Analog Input | Analog input 7, IDAC7. |
| 15 | REFN0 | Analog Input | Negative reference input 0. |
| 16 | REFP0 | Analog Input | Positive reference input 0. |
| 17 | REFN1 | Analog Input | Negative reference input 1. |
| 18 | REFP1/REFOUT | Analog Input | Positive reference input 1 or internal reference output. |
| 19 | AVSS | Analog | Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to –2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC. |
| 20 | AVDD | Analog | Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD. |
| 21 | CSn | Digital Input | Serial chip select. Active low. |
| 22 | DIN | Digital Input | Serial data input. |
| 23 | SCLK | Digital Input | Serial data clock. |
| 24 | DOUT/DRDYn | Digital Output | Serial data output and data ready indicator. |

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKING OPTION |
|---|---|---|---|---|
| SIG16130 | TSSOP-16 | -40°C to +125°C | SIG16130-ITSP16-RL | Reel, 5000 |
| SIG16131 | TSSOP-20 | -40°C to +125°C | SIG16131-ITSP20-RL | Reel, 4500 |
| SIG16132 | TSSOP-24 | -40°C to +125°C | SIG16132-ITSP24-RL | Reel, 3000 |

# SPECIFICATIONS

## Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | AVDD to AVSS | –0.3 | 6.5 | V |
| | AVSS to DGND | –3 | 0.3 | V |
| | DVDD to DGND | –0.3 | 6.5 | V |
| | Analog input | $V_{AVSS}$ – 0.3 | $V_{AVDD}$ + 0.3 | V |
| | Digital input | $V_{DGND}$ – 0.3 | $V_{DVDD}$ + 0.3 | V |
| Current | Input current | –10 | 10 | mA |
| Temperature | Junction ($T_J$) | –50 | 150 | °C |
| | Storage ($T_{stg}$) | -60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Ratings

| SYMBOL | PARAMTER | CONDITION | VALUE | UNIT |
|---|---|---|---|---|
| HBM | Human-body Model | ANSI/ESDA/JEDEC JS-001 | ±4000 | V |
| CDM | Charged-device model | JEDEC EIA/JS-002-2022 | ±2000 | V |

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at $V_{AVDD}$=5V, $V_{AVSS}$=0V, $V_{DVDD}$=3.3V, $V_{REF}$=2.5V, $f_{CLK}$=1.536MHz, data rate=10SPS, and PGA Gain=1, unless otherwise noted.

| PARAMETER | TEST CONDITION OR NOTES | MIN(1) | TYP | MAX(1) | UNITS |
|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | |
| Differential Input Voltage | $V_{IN} = V_{INP} – V_{INN}$ | $–V_{REF}$/Gain | | $+V_{REF}$/Gain | V |
| Absolute Input Voltage | PGA bypass | $V_{AVSS}$ – 0.05 | | $V_{AVDD}$ + 0.05 | V |
| | PGA enabled | $V_{AVSS}$ + 0.2 | | $V_{AVDD}$ – 0.2 | |
| Common MODE Input Range | PGA enabled | $V_{AVSS}$ + 0.2 + $\lvert V_{INMAX}\rvert$·Gain/2 | | $V_{AVDD}$ – 0.2 – $\lvert V_{INMAX}\rvert$·Gain/2 | V |
| Absolute Input Current | PGA bypass | | ±10 | | nA |
| | PGA enabled | | ±1 | | nA |
| **SYSTEM PERFORMANCE** | | | | | |
| PGA Gain | | | 1/2/4/8/16/32/ 64/128/256 | | V/V |
| Resolution | | | 16 | | Bits |
| Data Rate | | 2.5 | | 9600 | SPS |
| Noise | | | See Noise Table | | |
| Integral Nonlinearity (INL) | | | ±3 | | ppm |
| Offset Error | All PGA gains | | ±256/Gain | | µV |
| | After calibration | | In order of noise | | |
| Offset Drift vs. Temperature | All PGA gains | | ±256/Gain ± 3 | | nV/°C |
| Gain Error(2) | Gain=1 to 128 | -300 | ±100 | 300 | ppm |
| | Gain=256 | -450 | ±200 | 450 | ppm |
| Gain Mismatch(2) | Gain=1 to 128 | | 200 | 350 | ppm |
| Gain Drift vs. Temperature | All PGA gains | -3 | ±1 | 3 | ppm/°C |
| Normal MODE Rejection (NMRR) | $f_{IN}$=50/60Hz, ±2%, data rate=10SPS | | See Table 1 | | dB |
| Common MODE Rejection (CMRR) | $f_{IN}$=50/60Hz, data rate=1200SPS | 100 | 120 | | dB |
| Power Supply Rejection(2) (PSRR) | AVDD, AVSS | 75 | 90 | | dB |
| | DVDD | 80 | 120 | | dB |
| **EXTERNAL REFERENCE INPUT** | | | | | |
| Differential Reference Voltage ($V_{REF}$) | $V_{REF} = V_{REFP} – V_{REFN}$ | 0.5 | | $V_{AVDD} – V_{AVSS}$ + 0.1 | V |
| Absolute Negative Reference Voltage ($V_{REFN}$) | | $V_{AVSS}$ – 0.05 | | $V_{REFP}$ – 0.5 | V |
| Absolute Positive Reference Voltage ($V_{REFP}$) | | $V_{REFN}$ + 0.5 | | $V_{AVDD}$ + 0.05 | V |
| Average Voltage Input Current | | | 50 | | nA |
| **INTERNAL VOLTAGE REFERENCE** | | | | | |
| Reference Voltage | | | 2.5 | | V |
| Initial Accuracy | $T_A$ = 25˚C | -0.1% | ±0.01% | +0.1% | |
| Voltage Temperature Drift | $T_A$ = -40˚C to 125˚C | -20 | ±5 | +20 | ppm/°C |
| Power Supply Rejection | | | 90 | | dB |
| **EXCITATION CURRENT SOURCES** | | | | | |
| Output Current | $V_{REFP}$ = 2.5V | 10/50/100/200/250/500/1000 | | | µA |
| Compliance Voltage(3) | IDAC <= 250µA | $V_{AVSS}$ | | $V_{AVDD}$ – 0.5 | V |
| | IDAC = 500µA | $V_{AVSS}$ | | $V_{AVDD}$ – 0.6 | |
| | IDAC = 1000µA | $V_{AVSS}$ | | $V_{AVDD}$ – 0.8 | |
| Accuracy | IDAC =10µA | -4% | ±2% | +4% | |
| | IDAC >= 50µA | -2% | ±1% | +2% | |

| | | | | | |
|---|---|---|---|---|---|
| Current Mismatch | IDAC = 10μA | -3.0% | ±0.60% | +3.0% | |
| | IDAC = 50μA | -1.5% | ±0.25% | +1.5% | |
| | IDAC = 100μA | -1.2% | ±0.20% | +1.2% | |
| | IDAC = 200μA, 250μA | -1.0% | ±0.18% | +1.0% | |
| | IDAC = 500μA | -0.8% | ±0.12% | +0.8% | |
| | IDAC = 1000μA | -0.6% | ±0.1% | +0.6% | |
| Temperature Drift | | -90 | ±20 | +90 | ppm/°C |
| Temperature Drift Mismatch | | -30 | ±5 | +30 | ppm/°C |
| **BURNOUT CURRENT SOURCES** | | | | | |
| Current Setting | | | 1 | | μA |
| **TEMPERATURE SENSOR** | | | | | |
| Output Voltage | | | 113.3 | | mV |
| Temperature Coefficient | | | 377.6 | | uV/°C |
| **ADC CLOCK** | | | | | |
| External Clock | Frequency Range | 1 | 1.536 | 1.6 | MHz |
| | Duty Cycle | 40% | | 60% | |
| Internal Oscillator | Nominal Frequency | | 1.536 | | MHz |
| | Accuracy | –2% | ±0.5% | +2% | |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| High-level Output Voltage ($V_{OH}$) | $I_{OH}$ = 4mA | $0.8 \cdot V_{DVDD}$ | | | V |
| Low-level Output Voltage ($V_{OL}$) | $I_{OL}$ = –4mA | | | $0.2 \cdot V_{DVDD}$ | V |
| High-level Input Voltage ($V_{IH}$) | | $0.7 \cdot V_{DVDD}$ | | $V_{DVDD}$ | V |
| Low-level Input Voltage ($V_{IL}$) | | $V_{DGND}$ | | $0.3 \cdot V_{DVDD}$ | V |
| Input Hysteresis | | | 0.5 | | V |
| Input Leakage | | | | ±10 | μA |
| **POWER SUPPLY** | | | | | |
| AVSS Voltage ($V_{AVSS}$) | | –2.625 | | 0 | V |
| AVDD Voltage ($V_{AVDD}$) | | $V_{AVSS}$ + 2.7 | | $V_{AVSS}$ + 5.25 | V |
| DVDD Voltage ($V_{DVDD}$) | | 2.7 | | 5.25 | V |
| AVDD, AVSS Current ($I_{AVDD}$) | Buffer Off | | 250 | 350 | μA |
| | Buffer On | | 600 | 750 | μA |
| | Sleep MODE | | 1 | | μA |
| DVDD Current ($I_{DVDD}$) | Active MODE | | 180 | 300 | μA |
| | Sleep MODE | | 40 | | μA |
| Total Power Dissipation | Buffer Off | | 1.9 | | mW |
| | Buffer On | | 3.6 | | mW |
| | Sleep MODE | | 0.13 | | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified temperature range | | –40 | | 105 | °C |
| Operating temperature range | | –50 | | 125 | °C |
| Storage temperature range | | –60 | | 150 | °C |

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) Power supply rejection is specified DC change in voltage.
(3) The IDAC current does not change by more than 0.01% from the nominal value when staying within the specified compliance voltage.

## Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

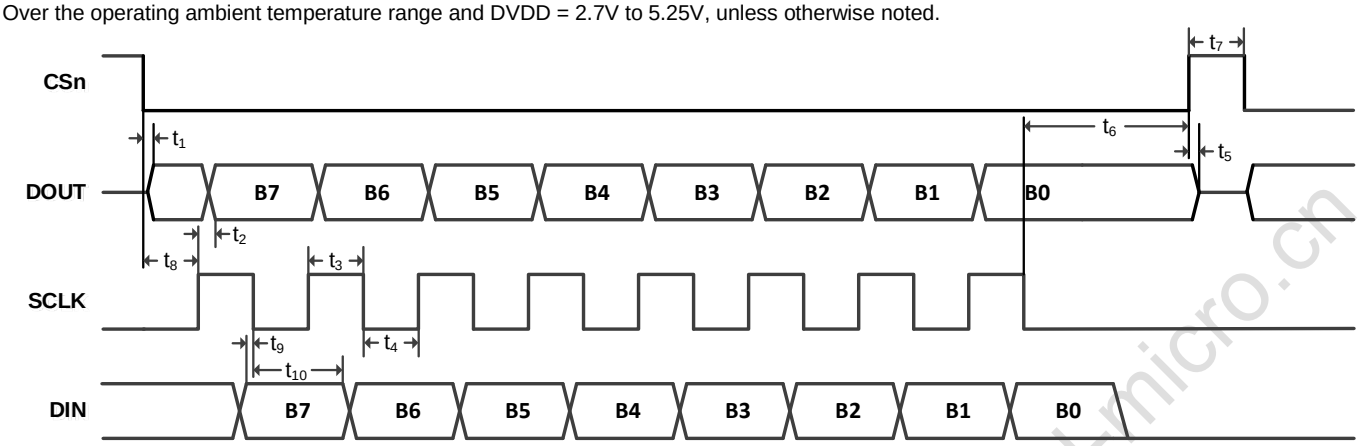



**Figure 1. Serial Interface Timing Requirements**

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_1$ | CSn falling edge to DOUT/DRDYn driven: propagation delay(1) | | 50 | ns |
| $t_2$ | SCLK rising edge to valid DOUT/DRDYn: propagation delay(1) | | 50 | ns |
| $t_3$ | SCLK high pulse width | 100 | | ns |
| $t_4$ | SCLK low pulse width | 100 | | ns |
| | SCLK period | 200 | $10^6$ | ns |
| $t_5$ | CSn rising edge to DOUT high impedance: propagation delay | | 40 | ns |
| $t_6$ | Last SCLK falling edge to CSn rising edge: delay time | 50 | | ns |
| $t_7$ | CSn high pulse width | 50 | | ns |
| $t_8$ | CSn falling edge to first SCLK rising edge: setup time(2) | 50 | | ns |
| $t_9$ | Valid DIN to SCLK falling edge: setup time | 50 | | ns |
| $t_{10}$ | Valid DIN to SCLK falling edge: hold time | 25 | | ns |

(1) DOUT load = 20pF || 100kΩ to DGND.
(2) CSn can be tied low.

## NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC4 and SINC1 filters. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF} / \text{Gain} / V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF} / \text{Gain} / V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

**Table 1. ADC Noise in μVRMS (μVPP) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 2.5 V, SINC4 Filter**

| Data Rate (SPS) | PGA GAIN | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 |
| 2.5 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 5 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 10 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 12.5 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 15 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 20 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 25 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 30 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 40 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 50 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 60 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.322) |
| 80 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.372) |
| 100 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.416) |
| 120 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.462) |
| 160 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.615) | 0.298(0.511) |
| 200 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.705) | 0.298(0.701) |
| 240 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.770) | 0.298(0.669) |
| 250 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.865) | 0.298(0.706) |
| 300 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.889) | 0.298(0.850) |
| 400 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(1.09) | 0.298(1.25) |
| 480 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.60) | 0.596(1.02) | 0.298(1.14) |
| 500 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.42) | 0.596(1.19) | 0.298(1.04) |
| 600 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.47) | 0.596(1.31) | 0.298(1.36) |
| 800 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.79) | 1.19(1.77) | 0.596(1.92) | 0.298(1.45) |
| 1000 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(3.33) | 1.19(2.15) | 0.596(1.96) | 0.298(1.74) |
| 1200 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.83) | 2.38(3.44) | 1.19(2.66) | 0.596(2.27) | 0.303(1.95) |
| 2000 | 76.3(76.3) | 38.1(39.7) | 19.1(23.6) | 9.54(10.2) | 4.77(6.70) | 2.38(4.71) | 1.19(3.89) | 0.596(2.94) | 0.390(2.93) |
| 2400 | 76.3(76.3) | 38.1(38.1) | 19.1(21.9) | 9.54(12.9) | 4.77(6.52) | 2.38(4.78) | 1.19(3.17) | 0.596(3.17) | 0.421(3.21) |
| 4000 | 76.3(213) | 38.1(120) | 19.1(55.7) | 9.54(28.2) | 4.77(16.2) | 2.38(9.73) | 1.19(6.37) | 0.649(4.77) | 0.565(4.17) |
| 4800 | 76.3(223) | 38.1(122) | 19.1(64.2) | 9.54(30.8) | 4.77(17.2) | 2.38(9.36) | 1.19(5.90) | 0.664(5.00) | 0.588(4.82) |
| 8000 | 311(3520) | 154(1140) | 79.1(730) | 38.7(380) | 19.2(163) | 9.88(82.2) | 4.94(37.4) | 2.56(18.0) | 1.44(11.2) |
| 9600 | 307(2690) | 156(1370) | 77.9(623) | 39.1(368) | 19.9(180) | 9.79(88.5) | 5.14(41.9) | 2.53(17.6) | 1.48(11.1) |

**Table 2. ADC ENOB (Noise Free Bits) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 5 V, SINC4 Filter**

| Data Rate (SPS) | PGA GAIN | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 |
| 2.5 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 5 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 10 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 12.5 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 15 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 20 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 25 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 30 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 40 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 50 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 60 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 80 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 100 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 120 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 160 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 200 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.9) |
| 240 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.7) |
| 250 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.6) |
| 300 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.8) |
| 400 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.3) |
| 480 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.8) | 16.0(15.3) |
| 500 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(12.3) |
| 600 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.9) | 16.0(15.1) |
| 800 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.5) | 16.0(14.6) |
| 1000 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.1) | 16.0(14.3) |
| 1200 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.3) | 16.0(14.3) |
| 2000 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.4) | 16.0(14.8) | 16.0(13.9) |
| 2400 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.5) | 16.0(14.6) | 16.0(13.8) |
| 4000 | 16.0(14.5) | 16.0(14.3) | 16.0(14.3) | 16.0(14.6) | 16.0(14.2) | 16.0(14.1) | 16.0(14.2) | 16.0(13.8) | 16.0(13.2) |
| 4800 | 16.0(14.4) | 16.0(14.1) | 16.0(14.3) | 16.0(14.3) | 16.0(14.2) | 16.0(14.2) | 16.0(14.1) | 16.0(13.8) | 15.9(13.0) |
| 8000 | 14.0(11.0) | 14.0(11.1) | 14.0(10.9) | 14.0(10.8) | 14.0(10.8) | 14.0(10.6) | 14.0(10.7) | 13.9(10.9) | 13.9(11.1) |
| 9600 | 13.9(10.2) | 14.0(10.9) | 14.0(10.7) | 13.9(10.8) | 14.0(10.9) | 14.0(11.0) | 14.0(10.8) | 13.9(11.0) | 13.9(10.9) |

**Table 3. ADC Noise in μVRMS (μVPP) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 2.5 V, SINC1 Filter**

| Data Rate (SPS) | PGA GAIN | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 |
| 2.5 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 5 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 10 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 12.5 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 15 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 20 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 25 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 30 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 40 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 50 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.298) |
| 60 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.316) |
| 80 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.596) | 0.298(0.365) |
| 100 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.622) | 0.298(0.601) |
| 120 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.719) | 0.298(0.659) |
| 160 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(0.821) | 0.298(0.941) |
| 200 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.19) | 0.596(1.05) | 0.298(1.00) |
| 240 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.32) | 0.596(1.03) | 0.298(0.958) |
| 250 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.54) | 0.596(1.02) | 0.298(1.46) |
| 300 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.44) | 0.596(1.41) | 0.298(1.42) |
| 400 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.48) | 1.19(1.43) | 0.596(1.63) | 0.298(1.29) |
| 480 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.38) | 1.19(1.98) | 0.596(1.62) | 0.298(1.27) |
| 500 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.97) | 1.19(2.18) | 0.596(1.61) | 0.298(1.45) |
| 600 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(2.66) | 1.19(1.86) | 0.596(2.04) | 0.298(1.79) |
| 800 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(9.54) | 4.77(4.77) | 2.38(3.57) | 1.19(2.46) | 0.596(1.99) | 0.311(1.94) |
| 1000 | 76.3(76.3) | 38.1(38.1) | 19.1(19.1) | 9.54(10.4) | 4.77(5.67) | 2.38(3.43) | 1.19(2.44) | 0.596(2.44) | 0.333(2.09) |
| 1200 | 76.3(76.3) | 38.1(38.1) | 19.1(19.5) | 9.54(10.0) | 4.77(6.06) | 2.38(3.86) | 1.19(2.73) | 0.596(2.47) | 0.371(2.31) |
| 2000 | 76.3(76.3) | 38.1(38.1) | 19.1(21.0) | 9.54(11.2) | 4.77(6.92) | 2.38(4.93) | 1.19(3.48) | 0.596(2.77) | 0.376(2.58) |
| 2400 | 76.3(76.3) | 38.1(38.1) | 19.1(25.2) | 9.54(12.0) | 4.77(7.66) | 2.38(4.34) | 1.19(3.63) | 0.596(3.03) | 0.421(2.90) |
| 4000 | 76.3(216) | 38.1(128) | 19.1(62.4) | 9.54(32.7) | 4.77(18.9) | 2.38(8.85) | 1.19(6.04) | 0.635(4.56) | 0.556(4.20) |
| 4800 | 76.3(303) | 38.1(136) | 19.1(57.2) | 9.54(34.3) | 4.77(18.0) | 2.38(9.36) | 1.19(6.55) | 0.673(5.32) | 0.584(4.56) |
| 8000 | 309(2690) | 158(1320) | 78.1(777) | 40.0(451) | 19.6(200) | 9.89(95.6) | 4.92(45.6) | 2.55(22.0) | 1.43(12.0) |
| 9600 | 311(3540) | 157(1660) | 78.1(754) | 38.7(318) | 19.6(213) | 9.88(80.8) | 4.96(36.3) | 2.55(19.5) | 1.44(10.9) |

**Table 4. ADC ENOB (Noise Free Bits) at $T_A$ = 25°C, $V_{AVDD}$ = 5 V, $V_{AVSS}$ = 0 V, $V_{REF}$ = 5 V, SINC1 Filter**

| Data Rate (SPS) | PGA GAIN | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 |
| 2.5 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 5 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 10 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 12.5 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 15 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 20 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 25 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 30 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 40 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 50 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 60 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 80 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 100 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) |
| 120 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.7) |
| 160 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.5) |
| 200 | 16.0(16.0) | 16.0(16.0) | 15.3(11.6) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.4) |
| 240 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.1) |
| 250 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.9) | 16.0(15.1) |
| 300 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.1) |
| 400 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.8) | 16.0(14.8) |
| 480 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.7) | 16.0(14.6) |
| 500 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.4) | 16.0(14.5) |
| 600 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.4) | 16.0(14.3) |
| 800 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.9) | 16.0(15.0) | 16.0(14.2) |
| 1000 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.7) | 16.0(15.2) | 16.0(14.2) |
| 1200 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.8) | 16.0(14.9) | 16.0(14.1) |
| 2000 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.5) | 16.0(14.7) | 16.0(13.7) |
| 2400 | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(16.0) | 16.0(15.2) | 16.0(14.7) | 16.0(13.6) |
| 4000 | 16.0(14.0) | 16.0(14.6) | 16.0(14.7) | 16.0(14.1) | 16.0(14.1) | 16.0(13.7) | 16.0(14.3) | 16.0(13.9) | 16.0(13.0) |
| 4800 | 16.0(14.3) | 16.0(14.5) | 16.0(14.0) | 16.0(14.4) | 16.0(14.0) | 16.0(14.0) | 16.0(14.0) | 16.0(13.9) | 15.9(13.1) |
| 8000 | 13.9(10.8) | 13.9(10.5) | 14.0(10.9) | 13.9(10.9) | 14.0(10.8) | 13.9(10.5) | 14.0(10.9) | 13.9(10.9) | 13.9(11.0) |
| 9600 | 14.0(10.9) | 14.0(11.0) | 13.9(10.9) | 14.0(11.0) | 13.9(10.5) | 13.9(10.5) | 13.9(10.8) | 13.9(10.7) | 13.9(10.7) |

## REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| July 12, 2022 | | Initial release. |

## DISCLAIMER

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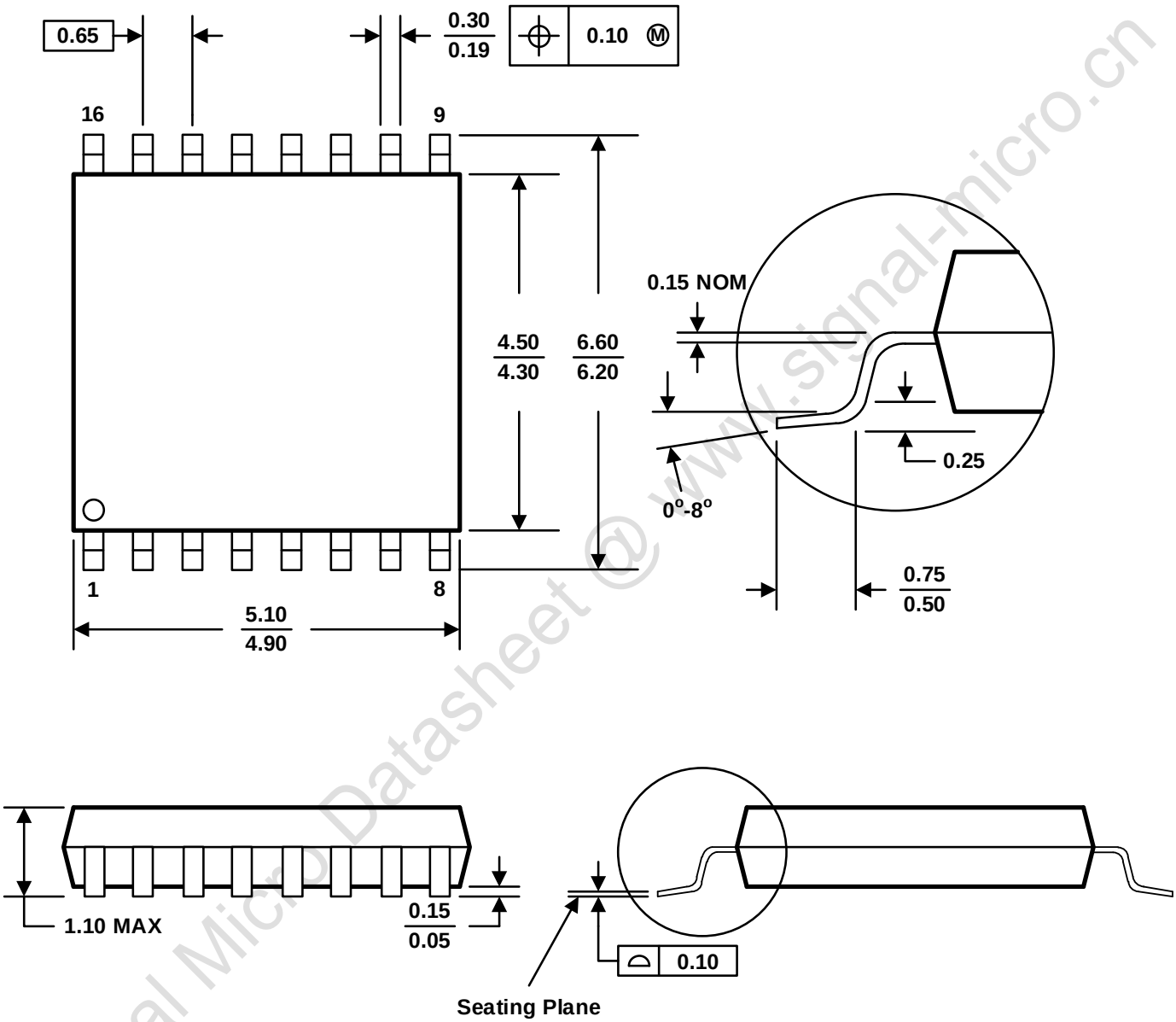
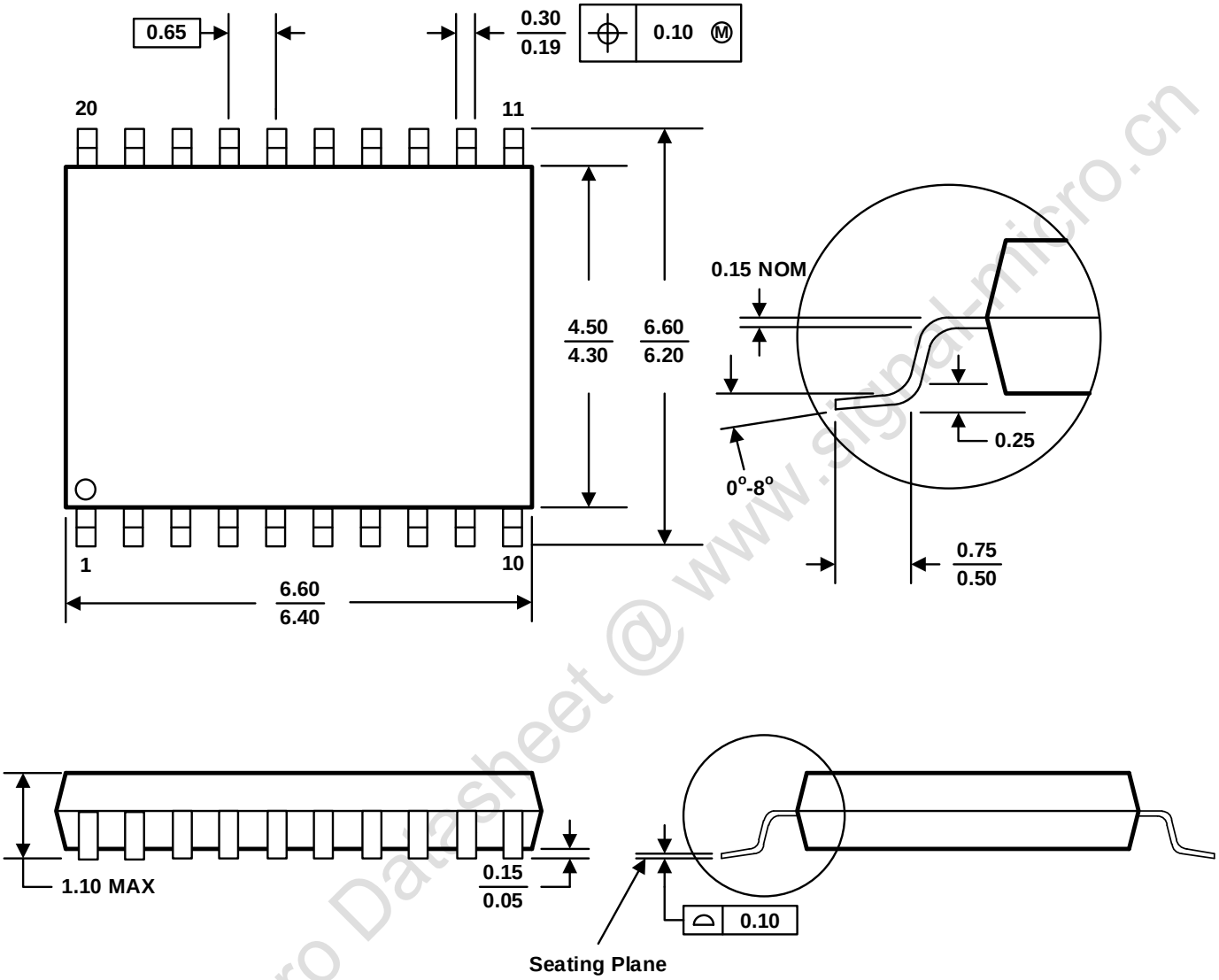
## PACKAGE OUTLINE DIMENSIONS

### TSSOP-16



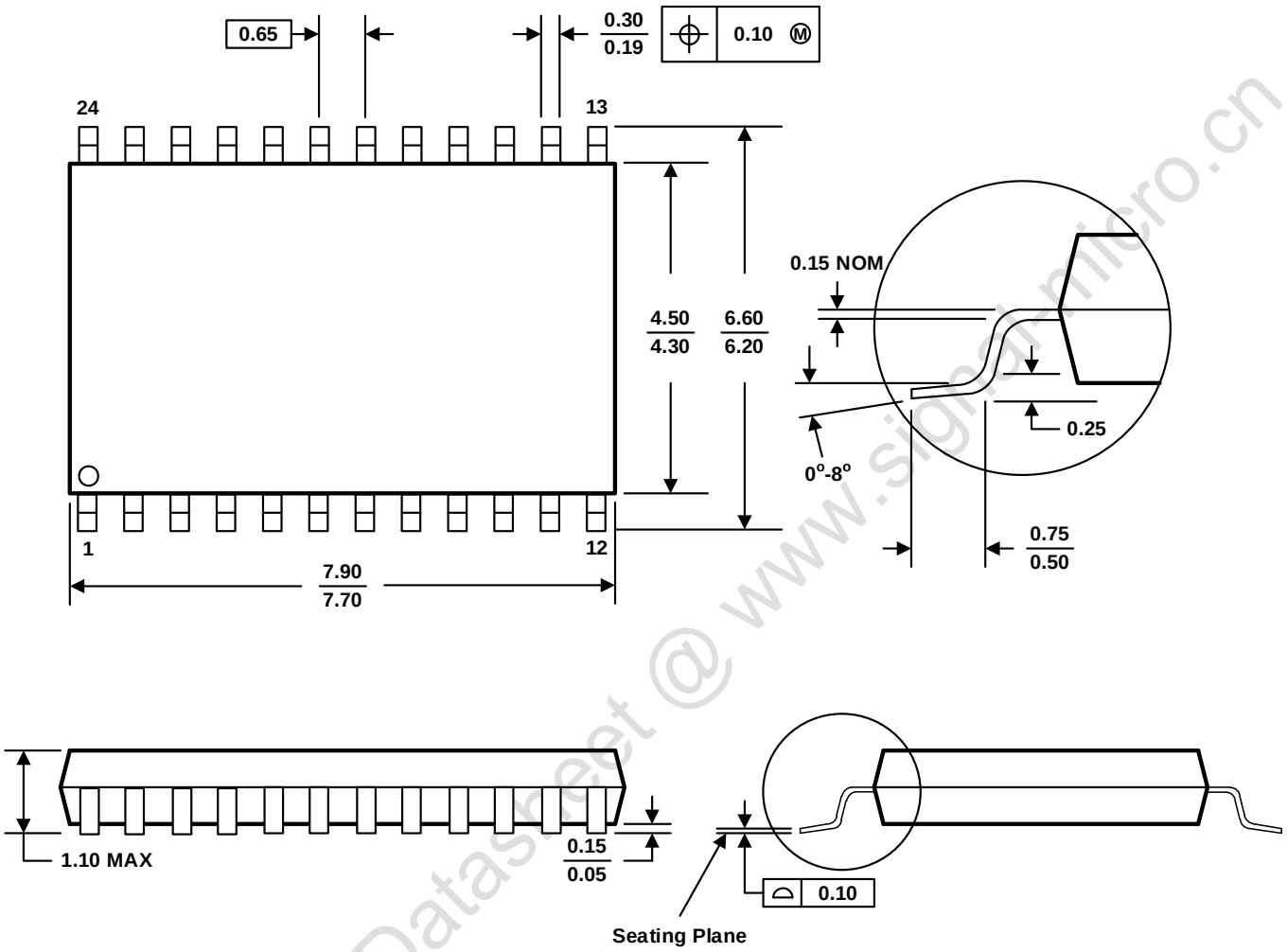

**A. Compliant to JEDEC STARDARDS MO-153-AD.**
**B. All linear dimensions are in millimeters.**
**C. This drawing is subject to change without notice.**

## TSSOP-20




**A. Compliant to JEDEC STARDARDS MO-153-AD.**
**B. All linear dimensions are in millimeters.**
**C. This drawing is subject to change without notice.**

## TSSOP-24




A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.